Attorney Docket No.: YOR920030249US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re PATENT APPLICATION of:

Jude A. RIVERS

Appln. No.:

Unknown

Art Unit:

Filed:

herewith

Examiner: Unknown

For:

DISTRIBUTED BUFFER INTEGRATED |
CACHE MEMORY ORGANIZATION |
AND METHOD OF REDUCING ENERGY |
CONSUMPTION THEROF

INFORMATION DISCLOSURE STATEMENT

Mail Stop PATENT APPLICATION Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir,

Pursuant to the duty of disclosure under 37 C.F.R. §1.56, submitted herewith is an Information Disclosure Statement (IDS) including copies of two (2) non patent references listed on a Form PTO-1449.

Since this IDS is being submitted with the application and prior to a first office action, no certification or fee is believed required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to all documents submitted. Consideration of the submitted documents is respectfully requested.

Respectfully Submitted,

August 20, 2003

(Date)

Charles W. Peterson, Jr. Registration No. 34,406

Customer Number 33233 Law Office of Charles W. Peterson, Jr. P.O. Box 710627 Oak Hill, VA. 20171 Tel.:(703)481-0532 Fax.:(703)481-0585

PTO/SB/08A (10-01)

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INFORMATION DISCLOSURE				Application Number		
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STATEMENT BY APPLICANT			ICANT	First Named Inventor	Rivers	
j				Art Unit		
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Sheet	1	of	2	Attorney Docket Number	YOR920030249US1	

	U.S. PATENT DOCUMENTS							
Examiner	Cite No.1	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where			
Initials*		Number - Kind² (if known)	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevan Figures Appear			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number		
				Filing Date		
				First Named Inventor	Rivers	
				Art Unit		
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Sheet 2 of 2		Attorney Docket Number	YOR920030249US1			

OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS							
Examiner Initials*	Cite No. Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, pate(s), volume-issue number(s), publisher, city and/or country where published.						
_		M ZHANG AND K. ASANOVICH, Highly Associative Caches for Low-Power Processors, Kool Chips Workshop, 33rd Int'l Symposium on Microarchitecture, , Published in: US					
		JUCE A. RIVERS, Performanceof High-Bandwidth Multi-Lateral Cache Organizations, 4/1/1998, Page(s) 143-147					

Examiner	Date		
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